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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,020	10/31/2000	Thomas Patrick Dawson	M-9050 US	9060

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EXAMINER

TRAN, TAM D

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/703,020

Applicant(s)

DAWSON, THOMAS PATRICK

Examiner

Tam D Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 17-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15, 17-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-15, 17-41, are rejected under 35 U. S.C. 103(a) as being unpatentable over Chauvin et al (USPN 5886701) in view of Bossut (USPN 6239807 B1), hereinafter simply Chauvin and Bossut.

2. In regard to claims 1, 17, Chauvin teaches a system and method for managing texture data, the system comprising: a texture memory controller (texture cache control) coupled to a texturing engine (texture filter engine); and a texture memory (texture cache) coupled to the texture memory controller, see Fig.9C, the texture memory configured to store texture data in a texture map set, the texture map set comprising two or more texture layers (transferring level of detail of the hi and lo MIP map levels to texture cache), see col.65 lines 20-27, wherein the texture memory controller is configured to access data from the texture memory and pass the data to the texturing engine. See col.5 lines 50-67, col.22 lines 52-56. Chauvin does not teach data is in a form of packet having at least two or more layers. However, Bossut teaches texture data including two layers having loading capability corresponding to a packet including two layers. See col.11 lines 1-10. It would have been obvious to a person of ordinary skill in the art at

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the time of the invention to incorporate the texture layers of Bossut into the texture engine of Chauvin because the combination of texture layer of Bossut and texture engine of Chauvin would provide the multi resolution texture mapping for an object. see col.2 lines 44-50.

3. In regard to claims 2, 21 Chauvin teaches a system for managing texture data, wherein a packet comprises color values associated with one color, the color values being from two or more texture layers. See col.5 lines 65-67.

4. In regard to claims 3, 22, Chauvin teaches a system for managing texture data, wherein the packet further comprises alpha values representing the amount of blending of the color values. See col.20 lines 52-60.

5. In regard to claims 4, 23, Chauvin teaches a system for managing texture data, wherein a packet comprises: a first red-green-blue texel from a first texture layer; and a second red-green-blue texel from a second texture layer. See col.63 lines 23-35.

6. In regard to claims 5, 24, Chauvin teaches a system for managing texture data, wherein the packet further comprises: a first alpha value associated with the first red-green-blue texel from the first texture layer; and a second alpha value associated with the second red-green-blue texel from the second texture layer. See col.63 lines 23-35.

7. In regard to claims 6, 25, Chauvin teaches a system for managing texture data, wherein the packet further comprises: a first red alpha value, a first green alpha value and a first blue alpha value associated with the first red-green-blue texel from the first texture layer; and a second red alpha value, a second green alpha value and a second blue alpha value associated with the second red-green-blue texel from the second texture layer. See col.67 lines 35-52.

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8. In regard to claims 7, 26, 35, Chauvin teaches a system for managing texture data, wherein the texturing engine is configured to modify the alpha values for one or more colors without modifying the alpha values for other colors. See col.19 lines 34-38.

9. In regard to claim 8, Chauvin teaches a system for managing texture data, further comprising a texture cache coupled to the texture memory controller and the texturing engine, the texture cache configured to store packets that have been recently retrieved from the texture memory, the texture cache configured to send recently-retrieved packets to the texturing engine. See col.5 lines 50-67.

10. In regard to claims 9, 20, Chauvin teaches a system for managing texture data, further comprising a set of texture cache status registers coupled to the texture memory controller and the texture engine, the texture cache status registers configured to store at least one texture attribute associated with the packets stored in the texture cache. See col.32 lines 25-50.

11. In regard to claims 10, 19, Chauvin teaches a system for managing texture data, wherein the texture memory is configured to store attributes associated with each texture layer, the attributes comprising: a width of a texture layer; a height of a texture layer; a texel format; and a texel packing factor. See col.48 lines 39-50.

12. In regard to claims 11, Chauvin teaches a system for managing texture data, wherein the texel format indicates the number of bits per texel, a texel operation mode, and a texture mode flag to indicate whether depth texturing is to be used or not. See col.63 lines 25-35.

13. In regard to claim 12, Chauvin teaches a system for managing texture data, wherein the texel packing factor is used by the texturing engine to layer several textures together for depth texturing. See col.63 lines 30-35.

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14. In regard to claim 13, Chauvin teaches a system for managing texture data, wherein the texel packing factor is used by the texturing engine to layer several textures together for combining several textures in a single rendering pass. See col.67 lines 45-50.

15. In regard to claim 14, Chauvin teaches a system for managing texture data, wherein the texture memory further comprises an alpha map, the alpha map comprising alpha values, each alpha value represents the amount of blending for a red-green-blue triplet within the texture memory. See col.54 lines 30-45.

16. In regard to claim 15, Chauvin teaches a system for managing texture data, wherein the texture memory further comprises an alpha map, the alpha map comprising alpha values, each alpha value represents the amount of blending of one color value in a texture layer within the texture memory. See col.54 lines 30-45.

17. In regard to claim 18, Chauvin teaches a system for managing texture data, further comprising: receiving a request for one or more packets; accessing a set of texture cache status registers to determine whether some or all of the requested packets are stored in a texture cache; passing requested packets stored in the texture cache to a texturing engine if some or all of the requested packets are stored in the texture cache; and retrieving requested packets from the texture memory if the texture cache does not have all of the requested packets. See col.5 lines 50-67.

18. In regard to claim 27, 40, Chauvin teaches a method of surface depth texturing, the method comprising: determining a depth stepping angle, see col. 63 lines 30-35, the depth stepping angle formed by a first vector from an eye point position to a fragment in a polygon surface and a second vector normal to the surface of the fragment; see col.64 lines 45-60;

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converting the depth stepping angle to one or more texel offset values; applying the texel offset values to a first texel in a first texture layer to find a corresponding second texel in a second texture layer; blending one or more color values and one or more alpha values associated with the first and second texels to create an apparent surface depth for the fragment; see col. 54 lines 31-47; and applying the blended color values and alpha values to the fragment. See col.63 lines 23-29.

19. In regard to claim 28, Chauvin teaches a method of surface depth texturing, wherein converting the depth stepping angle to one or more texel offset values comprises adjusting an amount of parallax between the first and second texture layers. See col.62 lines 47-50.

20. In regard to claim 29, Chauvin teaches a method of surface depth texturing, wherein adjusting an amount of parallax comprises left-shifting a set of binary bits representing the texel offset values. See col.63 lines 10-20.

21. In regard to claim 30, Chauvin teaches a method of surface depth texturing, further comprising right-shifting a set of binary bits representing the texel offset values by one bit for a selected second level MIP map, by two bits for a selected third level MIP map, by three bits for a selected fourth level MIP map. See col.63 lines 5-20.

22. In regard to claim 31, Chauvin teaches a method of surface depth texturing, wherein the texel offset values are positive. See col.63 lines 5-20.

23. In regard to claim 32, Chauvin teaches a method of surface depth texturing, wherein the texel offset values are negative. See col.63 lines 5-20.

24. In regard to claim 33, Chauvin teaches a method of surface depth texturing, wherein the color values comprise red, green and blue. See col.63 lines 25-30.

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25. In regard to claim 34, Chauvin teaches a method of surface depth texturing, wherein the alpha values comprise a red alpha value, a green alpha value and a blue alpha value. See col.63 lines 25-35.

26. In regard to claim 36, Chauvin teaches a method of surface depth texturing, wherein the alpha values from the second texel control blending of the first and second texel color values with an interpolated polygon color at a location of the fragment. See col.64 lines 20-30.

27. In regard to claim 37, Chauvin teaches a method of surface depth texturing, wherein the acts are repeated for a second fragment with a second depth stepping angle. See col.52 lines 50-65.

28. In regard to claim 38, Chauvin teaches a method of surface depth texturing, further comprising: caching the second texel and a third texel; and accessing a fourth texel from a texture memory and the third texel from a texture cache when the acts are repeated for a second fragment with a second depth stepping angle. See col.25 lines 25-49.

29. In regard to claim 39, Chauvin teaches a method of surface depth texturing, wherein the acts are preformed in real-time. See col.71 lines 10-15.

30. In regard to claim 41, Chauvin teaches a method of surface depth texturing, wherein each texel comprises a red color value, a red alpha value, a green color value, a green alpha value, a blue color value and a blue alpha value. See col.63 lines 25-35.

Response to Arguments

31. Applicant's arguments filed on 11/12/2003, have been fully considered but they are not persuasive.

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Applicant argues that the prior art does not teach “ texture memory configured to store texture data in a texture map set, texture map set comprising two or more texture layers”. However, examiner respectfully disagrees with the argument because on col.65 lines 20-27, Chauvin teaches the texture cache stores LOD (level of detail) for hi and lo MIP map levels corresponding to texture layers, and on col.11 lines 1-10, Bossut teaches texture data having layers. For these reasons, the rejections are maintained.


Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tam D. Tran** whose telephone number is **571-272-7793**. The examiner can normally be reached on MON-FRI from 8:30 – 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella** can be reached on **571-272-7778**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tam Tran

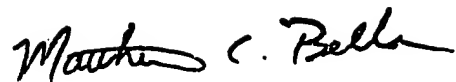

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A handwritten signature in black ink, reading "Matthew C. Bella". The signature is fluid and cursive, with the first name "Matthew" and last name "Bella" clearly distinguishable.

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600